LOW-COST X-BAND MIC PARAMETRIC AMPLIFIER

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Abstract

An X-band MIC parametric amplifier using planar printed circuit techniques which result in low-cost and high reliability has been developed. Design of a microstrip four-port circulator and parametric amplifier stage on a low-loss YIG substrate, a 31-GHz microstrip pump source on teflon-fiber glass, and a pump source at the same frequency in integrated fin-line are described.

Introduction

This paper reports on the computer-aided design and practical realization of an X-band microstrip parametric amplifier using planar MIC techniques which result in low cost and high reliability. The parametric amplifier employs a unique balanced circuit configuration in which a pair of low parasitic varactor chips are shunt-mounted in a low-loss YIG substrate[1]. The parametric amplifier is integrated with a four-port circulator[2, 3] also designed in microstrip with YIG as the dielectric substrate (Figure 1A). Use of YIG enables the circulator junction to be formed by an appropriate metallization on the substrate surface and thus eliminates the usual "puck in aperture" construction required with nonmagnetic substrates. This offers the advantages of simple, low-cost fabrication and facilitates the ultimate construction of both parametric amplifier and circulator on a single substrate. The parametric amplifier stage operates in the 9.2 to 9.8 GHz range with a bandwidth in excess of 100 MHz. The gain and noise figure of the parametric amplifier stage are typically 14 and 2.5 dB, respectively. Pump power is coupled to the varactor chips through a resonant slot in the ground plane of the parametric amplifier circuit (Figure 1B). The parametric amplifier operates with 31-GHz pump power provided by a solid-state source which also is amenable to low-cost fabrication techniques. The source consists of a Gunn oscillator designed either in microstrip[4] or integrated fin-line[5], each using teflon-fiber glass as the dielectric substrate. The total integrated amplifier package, which includes the four-port circulator, parametric amplifier stage, and solid-state pump source, is particularly applicable for use in distributed array transmit-receive modules by virtue of its small size and low cost. A rigorous manufacturing and cost analysis of the amplifier package was performed which indicates that a unit price of less than $200 is realizable in production runs of 200,000.

Analysis And Results

Parametric Amplifier Stage

The parametric amplifier stage utilizes a matched pair of varactor chips shunt-mounted in a balanced configuration as shown in Figure 2. An idler frequency resonant circuit is associated with each varactor. It consists of the varactor chip itself and the high-impedance microstrip line Z_H of length D_I. This line is terminated in a virtual short circuit in plane A-A due to the circuit balance. Pump power is provided to the varactors through a resonant slot in the ground plane. The signal input circuit provides both reactive tuning and impedance transformation which jointly serve to establish the required gain level and operating bandwidth of the parametric amplifier. These are provided by the length D_S of high impedance line, Z_H and the quarterwave sections T_1 and T_2, respectively. The circuit equivalent of Figure 2 is shown in Figure 3 and forms the basis of the design analysis. The analysis was based on the following inputs:

• Signal center frequency	9.5 GHz
• Pump frequency	31.2 GHz
• Characteristic impedance of signal tuning line	80 ohms
• Characteristic impedance of input line	50 ohms
• Characteristic impedance of idler line	80 ohms
• Sum frequency loading	Open circuit
• Varactor chip junction capacitance (biased)	0.125 pF
• First order nonlinearity ratio of capacitance	0.21
• Second order nonlinearity ratio of capacitance	0.064
• Varactor chip parasitic capacitance	0.04 pF
• Varactor chip series resistance	3.0
• Varactor chip series inductance	0.08 nH

Computations yield the following circuit parameters:

• Length of idler line, D_I	13 mils
• Length of signal tuning line, D_S	28 mils
• Impedance of first quarter-wave section, T_1	37 ohms
• Impedance of second quarter-wave section, T_2	50 ohms
• Center frequency gain	14 dB

The details of the analysis are outlined in Figure 4 in the form of computer printouts. The first printout (Figure 4A) refers to the impedance in plane A-A of the signal circuit and demonstrates the broadband nature of the negative resistance characteristic and its symmetry with respect to the midband frequency. It also demonstrates the large capacitive reactance which exists in plane A-A and indicates that inductance is required to tune the signal circuit. This is provided by the length D_S of high-impedance line Z_H. The next computer printout (Figure 4B) shows the impedance in plane B-B for Z_H = 80 ohms and D_S = 28 mils. The reactance is essentially zero at midband and behaves with frequency as in a series resonant circuit. The negative resistance retains its broadband character and still peaks essentially at midband. Also shown is the gain characteristic which would result if the 50-ohm circulator were connected directly at plane B-B. The gain level is significantly below the design goal of 14 dB and hence impedance transformation is required to increase the magnitude of the negative resistance and thereby achieve higher gain at midband. This is accomplished by quarter-wave transformers T_1 and T_2. The third computer readout (Figure 4C) shows the impedance and gain characteristics in plane C-C for T_1 = 37 ohms and T_2 = 50 ohms. It is seen that the negative resistance levels are increased by the transformation and that the signal resonance still occurs at midband. The gain at midband is now at the design level of 14 dB.

An experimental gain characteristic is shown in Figure 5. It is in good qualitative agreement with the corresponding computed characteristic shown in Figure 4C. The results were achieved using matched pairs of unpackaged varactor chips shunt-mounted through two small diameter holes in the 20-mil thick YIG substrate. These chips were developed internally at AIL in the Central Research Group and exhibit zero bias capacitance of 0.175 + 0.025 pF and cutoff frequencies in excess of 300 GHz. The measured noise figure of the parametric amplifier stage is approximately 2.5 dB and was determined by the standard Y-factor method using a calibrated noise lamp.

Circulator

The basic circulator is a 50-ohm three-port circuit designed in microstrip using 20-mil thick YIG as the dielectric substrate. The design incorporates half-wave parallel resonators to achieve fixed-tuned, broadband operation. The small metallized tabs afford opportunity for fine tuning if required. At center band, the insertion loss is approximately 0.6 dB. The circulator exhibits 20-dB isolation when tuned to operate over the entire 9.2 to 9.8 GHz range. When tuned to accommodate narrower bands, the isolation can be peaked to higher levels, for example, 24 dB over 250 MHz and 27 dB over 150 MHz. The four-port circulator used in the final amplifier assembly is formed by the interconnection of 2 three-port circulator circuits.

Solid-State Pump Source

The basic configuration for the 31-GHz pump source consists of a single Gunn diode shunt-mounted in either a microstrip cavity or an integrated fin-line cavity. Bias is provided in each case through a simple MIC low-pass filter. Gunn diodes in chip form are not available at K_a-band and consequently packaged units have been used. The output power of the pump source is dependent upon the RF power rating of the Gunn diode. Typically, power levels within 2 dB of that obtained in rectangular waveguide cavities have been achieved in each of these MIC configurations.

Conclusion

The results summarized previously demonstrate the feasibility of realizing an X-band solid-state parametric amplifier using printed circuits in integrated form. By virtue of its small size and low cost, the integrated amplifier is particularly attractive for phased array applications. A detailed manufacturing and cost analysis indicates that a unit price of less than $200 is achievable in runs of 200,000.

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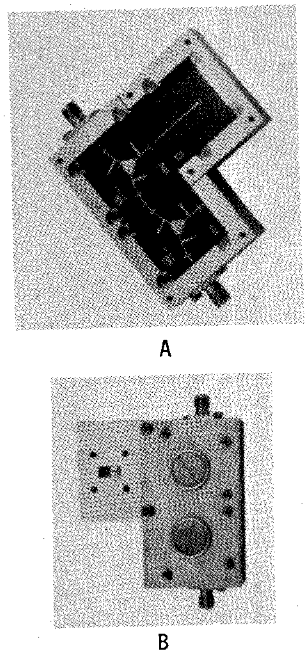


Fig. 1. Parametric amplifier stage and four-port circulator

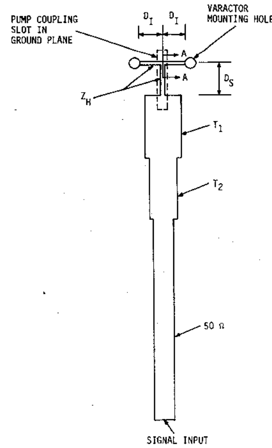
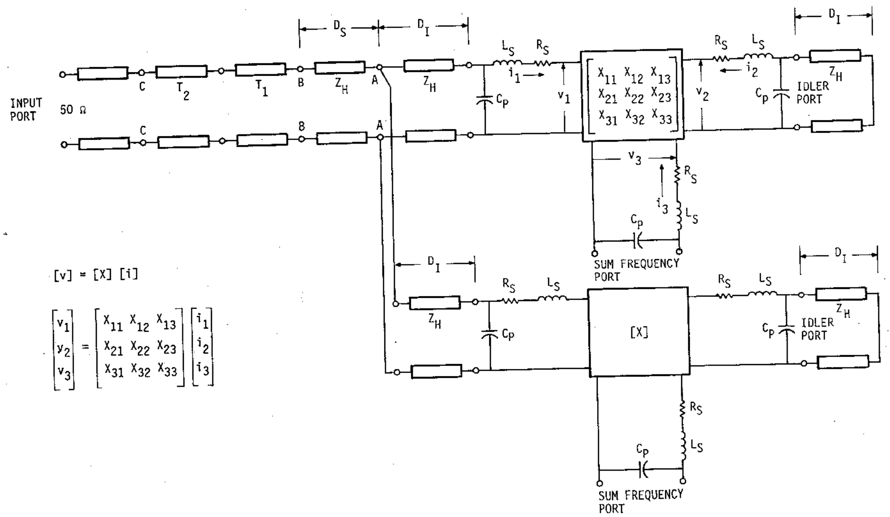


Fig. 2. Physical layout of balanced parametric amplifier



$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} X_{11} & X_{12} & X_{13} \\ X_{21} & X_{22} & X_{23} \\ X_{31} & X_{32} & X_{33} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix}$$

Fig. 3. Equivalent circuit of balanced parametric amplifier

4A

F SUB S(GHZ)	RPAR(OHMS)	XPAR(OHMS)
9.000	-8.791	-49.004
9.100	-11.235	-48.587
9.200	-14.295	-47.460
9.300	-17.735	-45.056
9.400	-20.751	-40.886
9.500	-22.049	-35.230
9.600	-20.854	-29.503
9.700	-17.806	-25.215
9.800	-14.230	-22.780
9.900	-11.025	-21.732
10.000	-8.473	-21.466

4B

F(GHZ)	G(DB)	R	X
9.000	2.160	-6.504	-11.239
9.100	2.785	-8.324	-10.718
9.200	3.615	-10.667	-9.772
9.300	4.667	-13.478	-7.987
9.400	5.822	-16.329	-4.865
9.500	6.654	-18.268	-0.252
9.600	6.580	-18.297	5.084
9.700	5.650	-16.378	9.749
9.800	4.468	-13.485	12.909
9.900	3.425	-10.606	14.681
10.000	2.611	-8.201	15.571

4C

F(GHZ)	G(DB)	R	X
9.000	3.412	-13.857	-31.869
9.100	4.485	-17.005	-28.136
9.200	5.997	-20.959	-23.755
9.300	8.156	-25.572	-18.068
9.400	11.151	-30.156	-10.366
9.500	13.993	-33.300	-0.460
9.600	12.789	-33.804	10.637
9.700	9.489	-31.298	21.064
9.800	6.870	-27.028	29.519
9.900	5.032	-22.429	35.943
10.000	3.744	-18.345	40.982

Fig. 4. Computer readouts corresponding to planes A-A, B-B, and C-C of Figure 3

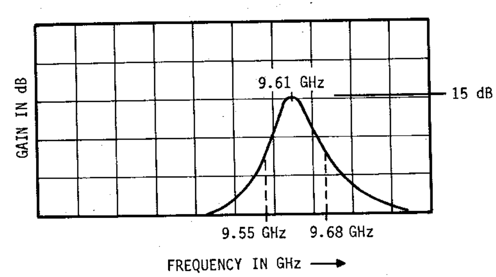


Fig. 5. Experimental gain versus frequency characteristic of parametric amplifier stage